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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,099	11/26/2003	Toshihiko Okamura	Q78646	6194

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EXAMINER	
RIZK, SAMIR WADIE	
ART UNIT	**PAPER NUMBER**
2133	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/721,099	OKAMURA ET AL.	
	Examiner	Art Unit	
	Sam Rizk	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 2/20/2007.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

GUY LAMARRE
PRIMARY EXAMINER

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 26 November 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

- Response to the applicant's amendment dated 2/20/2007
- Claims 1-22 have been submitted for examination
- Claims 1-22 have been rejected

Claim Rejections - 35 USC § 101

1. In view of the applicant-amended claim 17, all rejections to the claim 17 under section *35 USC § 101* are withdrawn.

Claim Objections

2. Claim 1 is objected to because of the following informalities:

Claim 1, line 11 should read "..permutation matrix ~~is~~ **of** said sub-matrix..".

Appropriate correction is required.

Priority

3. Should applicant desire to obtain the benefit of foreign priority under 35 U.S.C. 119(a)-(d) prior to declaration of an interference, a certified English translation of the foreign application must be submitted in reply to this action. 37 CFR 41.154(b) and 41.202(e).

Failure to provide a certified translation may result in no benefit being accorded for the non-English application.

Allowable Subject Matter

4. The indicated allowability of claims –1-22 is withdrawn in view of the newly discovered reference(s) to Zhang et al. US patent no. 7120856 (Hereinafter Zhang). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Zhang.

6. In regard to claim 1, Zhang teaches:

(currently amended): An error correcting code decoding device based on Message-Passing decoding on a Low-Density Parity-Check Code, whose parity-checkmatrix consists of sub-matrices of a Kronecker product of two permutation matrices (Note: col. 5, lines (51-67) through col. 6, lines (1-18) in Zhang), comprising:
a plurality of memory means (Fig. 6, RAMs (1,1) – (k,k) in Zhang) for storing a received value and a message generated during said decoding;
a plurality of variable node function means (Fig. 6, PE (1,1) – PE (k,k), note the VNU variable node units reference characters in Zhang) which perform variable node processing in said decoding;
a plurality of check node function means (Fig. 6, CNU's check node

units reference characters in Zhang) which perform check node processing in said decoding;
a plurality of address generation means (Fig. 4, AG (1,1) – AG (k,k) address generation reference characters in Zhang) for generating an address of said memory means on the basis of the first permutation matrix is said sub-matrix of a Kronecker product; and
a plurality of shuffle network means (Fig. 6, Pi (1) - Pi (3) shuffle networks in Zhang) for determining a connection between said variable node function means on the basis of the second permutation matrix in said sub-matrix of a Kronecker product;
wherein said check node functions(s) means perform(s) check node processing sequentially (The Examiner notes that CNU processing is performed sequentially from node (1,1) through (3,k) in Fig. 6, in Zhang) on a unit of said second permutation matrix, and said variable node functions generate messages in accordance with said current check node processing.
(Note; col. 8, lines (45-67) in Zhang)

7. In regard to claim 2, Zhang teaches:

(previously presented): The error correcting code decoding device according to claim 1, wherein said address generation means (Note; Fig. 4, AG(1,1) through AG (k,k) in Zhang) singly generate an address for all of said memory means; and
wherein said shuffle network means are singly connected to all of said variable node function means.
(Note: Fig. 4, reference character (402) in Zhang)

8. In regard to claim 3, Zhang teaches:

(previously presented): The error correcting code decoding device according to claim 1, wherein said memory means store said message with a sum thereof.
(Note col. 4, equations 2 and 3 in Zhang)

9. In regard to claim 4, Zhang teaches:

(previously presented): The error correcting code decoding device according to claim 1, wherein said address generation means are provided as a counter.
(Note: Fig. 3, reference character "counter" in Zhang)

10. In regard to claim 5, Zhang teaches:

(previously presented): The error correcting code decoding device according to claim 1, wherein a second permutation by said shuffle network means is determined on a basis of a Galois field calculation.
(Note: Fig. 6, reference characters Pi 1-3 in Zhang)

11. In regard to claim 6, Zhang teaches:

(previously presented): The error correcting code decoding device according to claim 1, wherein said decoding corrects a message of an output from said check node function means by multiplying the output by a coefficient less than 1 on a basis of a min-sum algorithm.
(Note: col. 4, EQ. (1) in Zhang)

12. In regard to claim 7, Zhang teaches:

(previously presented): The error correcting code decoding device according to claim 1, wherein in said decoding, said check node function means hold a first minimum value of an absolute value of an input message and an index thereof, and a second minimum value of the input message and information regarding whether the input message is positive or negative on a basis of a min-sum algorithm.
(Note: col. 6, lines (58 & 59) in Zhang)

13. In regard to claim 8, Zhang teaches:

(original): The error correcting code decoding device according to claim 1, wherein decoding on a different code is dealt with by changing only said address generation means.
(Note the decoder architecture of the LDPC (2,K) in col. 6, line 20 and (3,K) in col. 7, line 34 in Zhang)

14. In regard to claim 9, Zhang teaches:

(previously presented): The error correcting code decoding device according to claim 1, wherein decoding on a uniform Low-

Density Parity-Check Code is implemented by providing a function to always send a message that an output has a codeword bit with an extremely high probability of 0 to a set of said variable node function means corresponding to one of said address generation means and said shuffle network means.
(Note Fig. 7 in Zhang)

15. Claims 10 and 17 are rejected for the same reasons as per claim 1.

16. Claims 11 and 18 are rejected for the same reasons as per claim 3.

17. Claims 12 and 19 are rejected for the same reasons as per claim 5.

18. Claims 13 and 20 are rejected for the same reasons as per claim 6.

19. Claims 14 and 21 are rejected for the same reasons as per claim 7.

20. Claims 15 and 22 are rejected for the same reasons as per claim 8.

21. Claim 16 is rejected for the same reasons as per claim 9.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Rizk whose telephone number is (571) 272-8191. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronics Business Center (EBC) at 866-217-9197 (toll-free)

Sam Rizk, MSEE, ABD

Examiner

ART UNIT 2133

3/20/07